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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,422	02/05/2002	Tsuyoshi Yoneyama	111907	4116

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EXAMINER	
NGUYEN, KEVIN M	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,422	YONEYAMA, TSUYOSHI	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23,25 and 26* is/are rejected.

7)☒ Claim(s) *24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments, see interview summary, filed 12/13/2004, with respect to the final rejection of claims 1-26 and rejection under 112, second paragraph have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. An action follows below:

Information Disclosure Statement

2. The information disclosure statement filed 11/08/2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 8-12, 14-18 and 20-21 are rejected under 35 U.S.C. 103(a) as being anticipated by Kudo et al (previously cited, US 6,353,435) in view of Bassetti, Jr. (previously cited, US 5,122,783).

4. As to claim 1, Kudo et al teaches a display drive circuit comprising

a. a frame memory (8), figure 1, column 7, lines 29-3.

b. a plurality of grayscale pattern selection circuits, see figure 4, column 9, lines 33-38, is defined by gray-scale No. 1 pattern generator, gray-scale No. 2 pattern generator gray-scale No. 3 pattern generator,..., gray-scale No. N pattern generator, and 64 to 1 selector 108.

c. a plurality of frame selection circuits, see fig. 3, col. 9, lines 28-30, is defined by the FRC decoders 101 to 104, and a write data selector 106, with respect to the input gray-scale data of a pixel, generate indicate on/off data associated with the value of the gray-scale data. Accordingly, the gray-scale No.1-N pattern generators configure in one single FRC decoder. Thus, they are still provided in correspondence with each other.

d. the plurality of Frame Rate Control (FRC) decoder 101 to 104 configures and generate FRC pattern including the grayscale pattern (fig. 4) to be output at the N-th frame, col. 9, lines 52-57.

Accordingly, Kudo et al teaches all of the claimed limitations of claim 1, except for the Random Access Memory is electrically connected to (and based on) the plurality of gray scale pattern selection circuits.

However, Jr. Bassetti teaches Random Access Memory (RAM) (1080) (see fig. 10A) directly connects to (and based on) a plurality of gray scale pattern selected circuits is defined, recited at col. 17, lines 14-16, gray scale (G/S) selecting module 1090, a MOD-N G/S unit 800, a MOD-3 G/S unit 875, a MOD-2 G/S unit 870, and a MUX 1095 (see fig. 10A).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to substitute Kudo's frame memory (8) for RAM including directly connected to (and based on) the plurality of gray scale pattern selection units, in view of the teaching in Jr. Bassetti's reference because this would provide the weights to be attributed to each brightness level for realizing gamma correction or other brightness weighting functions as desired (col. 17, lines 11-13, Bassetti).

As to claim 2, Kudo et al teaches a data width converter 22 (an image data conversion circuit, fig. 2) which receives 6 bits data (N bits), converts the 6 bits data into 16 bits data (M bits, M>N) grayscale pattern (1 or 4F, 2 or 5F, 3 or 6F) and supplies the 16 bits data to frame memories A, B (8a, 8b) (figure 2, column 8, lines 16-25).

As to claims 3-4, Jr. Bassetti teaches Random Access Memory (RAM) (1080) (see fig. 10A) directly connects to (and based on) a plurality of gray scale pattern selected circuits is defined, recited at col. 17, lines 14-16, gray scale (G/S) selecting module 1090, a MOD-N G/S unit 800, a MOD-3 G/S unit 875, a MOD-2 G/S unit 870, and a MUX 1095 (see fig. 10A).

5. As to claim 5, Kudo et al teaches the plurality grayscale No. 1 to No. 64 pattern generator, and the selector 108 (fig. 4) (each of frame selection circuit is disposed one side of the corresponding grayscale pattern selection circuit, figure 4, column 10, lines 12-50).

Therefore, Kudo teaches all of the claimed limitation except for "each of frame selection circuit is divided into a plurality of portions that are disposed either side of the corresponding grayscale pattern selection circuit".

Absent a showing of criticality it would have been within the level of skill in the art and obvious to one having ordinary skill to engineering design to make separable (each of frame selector circuit is divided into a plurality of portions that are disposed either side) of a well-known element is normally not directed toward patentable subject matter as desired as was judicially recognized in *Nerwin v. Erlichman, 168 USPQ 177, 179 (PTO Bd. Of Int. 1969).*

6. As to claim 6, Kudo et al teaches a display drive circuit associated with a method, the display drive circuit comprising

e. a frame memory (8), figure 1, column 7, lines 29-31.

f. a plurality of grayscale pattern selection circuits, see figure 4, column 9, lines 33-38, is defined by gray-scale No. 1 pattern generator, gray-scale No. 2 pattern generator gray-scale No. 3 pattern generator,..., gray-scale No. N pattern generator, and 64 to 1 selector 108.

g. the FRC decoders 101 to 104 generated indicated on/off data for formation of an FRC pattern to be output at a frame previous by 2 frames each time the Vsync count value issued from the Vsync counter 105 (i.e. with mutually different frame cycles, see detailed in Fig. 5, col. 9, lines 64 through col. 10, line 1).

h. the 64 type of grayscale pattern generators of the FRC pattern generator 107 (fig. 4) of the FRC decoder 101 corresponding in number to the grayscale data bits are set to generate...to be output at the odd ones of frames included in

the FRC period (col. 10, lines 11-18), at the even ones of frame included in the FRC period (col. 10, lines 21-28).

i. the drive frame frequency to be output to the STN liquid crystal display (col. 15, lines 24-26) based on the grayscale pattern (see fig. 4) from FRC decoders 101 to 104 (see fig. 3).

Accordingly, Kudo et al teaches all of the claimed limitations of claim 6, except for the Random Access Memory is electrically connected to (and based on) the plurality of gray scale pattern selection circuits.

However, Jr. Bassetti teaches Random Access Memory (RAM) (1080) (see fig. 10A) directly connects to a plurality of gray scale pattern selected circuits is defined, recited at col. 17, lines 14-16, gray scale (G/S) selecting module 1090, a MOD-N G/S unit 800, a MOD-3 G/S unit 875, a MOD-2 G/S unit 870, and a MUX 1095 (see fig. 10A).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to substitute Kudo's frame memory (8) for RAM including directly connected to (and based on) the plurality of gray scale pattern selection units, in view of the teaching in Jr. Bassetti's reference because this would provide the weights to be attributed to each brightness level for realizing gamma correction or other brightness weighting functions as desired (col. 17, lines 11-13, Bassetti).

As to claim 7, Kudo et al teaches a data width converter 22 (an image data conversion circuit, fig. 2) which receives 6 bits data (N bits), converts the 6 bits data into

16 bits data (M bits, M>N) grayscale pattern (1 or 4F, 2 or 5F, 3 or 6F) and supplies the 16 bits data to frame memories A, B (8a, 8b) (figure 2, column 8, lines 16-25).

7. As to claims 8-13, Kudo et al teaches a liquid crystal controller (3) (a drive signal circuit), a liquid crystal display (9) (a terminal outputs a drive signal, figure 1, column 7, lines 25-37) based on the grayscale pattern (see fig. 4).

8. As to claims 14-19, Kudo et al teaches column drivers (504, 505), and row drivers (502, 503) (figure 48) which mutually intersect inherent pixels.

9. As to claim 20, Kudo et al teaches a display drive circuit associated with a method, the display drive circuit comprising

j. a selector 108 for selecting one of the 64 types of indicate on/off data generated by the FRC pattern generator 107 (col. 9, lines 36-38),

k. FRC pattern to be output at a frame previous by 2 frames each time, (having at least two types of frames cycles, fig. 5, col. 9, lines 65-66).

l. The 64 type of grayscale pattern generators of the FRC pattern generator 107 (fig. 4) of the FRC decoder 101 corresponding in number to the grayscale data bits are set to generate...to be output at the odd ones of frames included in the FRC period (col. 10, lines 11-18), at the even ones of frame included in the FRC period (col. 10, lines 21-28) (outputting the selected grayscale pattern for each frame).

m. the 12-bits parallel data of the upper and lower displays are output to the liquid crystal display 9 (col. 16, lines 42-43) (outputting a drive signal for driving a display portion).

Accordingly, Kudo et al teaches all of the claimed limitations of claim 20, except for "... based on data for image display stored in the Random Access Memory."

However, Jr. Bassetti teaches a plurality of gray scale pattern selected circuits [(gray scale (G/S) selecting module 1090, a MOD-N G/S unit 800, a MOD-3 G/S unit 875, a MOD-2 G/S unit 870, and a MUX 1095 (see fig. 10A)] based on Random Access Memory (RAM) (1080), see fig. 10A, recited at col. 17, lines 14-16.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to substitute Kudo's frame memory (8) for RAM including connected and based on the plurality of gray scale pattern selection units, in view of the teaching in Jr. Bassetti's reference because this would provide the weights to be attributed to each brightness level for realizing gamma correction or other brightness weighting functions as desired (col. 17, lines 11-13, Bassetti).

10. As to claim 21, Kudo et al teaches associated with a method, the display drive circuit comprising

a data width converter 22 (an image data conversion circuit, fig. 2) which receives 6 bits data (N bits), converts the 6 bits data into 16 bits data (M bits, M>N) grayscale pattern (1 or 4F, 2 or 5F, 3 or 6F) and supplies the 16 bits data to frame memories A, B (8a, 8b) (figure 2, column 8, lines 16-25).

11. Claims 22, 23, 25 and 26 are rejected under 35 U.S.C. 103(a) as being anticipated by Kudo et al in view of Jr. Bassetti, and further in view of Hirai et al (newly cited, US 5,953,002).

12. As to claim 22, Kudo et al teaches a display drive circuit associated with a method, the display drive circuit comprising

n. a frame memory (8), figure 1, column 7, lines 29-31.

o. a plurality of grayscale pattern selection circuits, see figure 4, column 9, lines 33-38, is defined by gray-scale No. 1 pattern generator, gray-scale No. 2 pattern generator gray-scale No. 3 pattern generator,..., gray-scale No. N pattern generator, and 64 to 1 selector 108.

p. the FRC decoders 101 to 104 generated indicated on/off data for configuration of an FRC pattern to be output at a frame previous by 2 frames each time the Vsync count value issued from the Vsync counter 105 (i.e. with mutually different frame cycles, see detailed in Fig. 5, col. 9, lines 64 through col. 10, line 1).

q. a plurality of frame selection circuits, see fig. 3, col. 9, lines 28-30, is defined by the FRC decoders 101 to 104, and a write data selector 106.

r. The plurality of Frame Rate Control (FRC) decoders 101 to 104 configures and generates FRC pattern including grayscale pattern to be output at the N-th frame, N+1-th frame, N+2-th frame, and N+3-th frame (col. 9, lines 55-63).

s. Accordingly, the drive frame frequency including grayscale pattern (fig. 7), and the FRC patterns A to D are made up of indicate display on/off data issued from the FRC decoders 101 to 104 (fig. 7, col. 11, lines 1-7) to be output to the STN liquid crystal display 9 (fig. 1, col. 15, lines 24-25).

Accordingly, Kudo et al teaches all of the claimed limitations of claim 22, except for the Random Access Memory is electrically connected to (and based on) the plurality of gray scale pattern selection circuits.

However, Jr. Bassetti teaches Random Access Memory (RAM) (1080) (see fig. 10A) directly connects to (and based on) a plurality of gray scale pattern selected circuits is defined, recited at col. 17, lines 14-16, gray scale (G/S) selecting module 1090, a MOD-N G/S unit 800, a MOD-3 G/S unit 875, a MOD-2 G/S unit 870, and a MUX 1095 (see fig. 10A).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to substitute Kudo's frame memory (8) for RAM including directly connected to (and based on) the plurality of gray scale pattern selection units, in view of the teaching in Jr. Bassetti's reference because this would provide the weights to be attributed to each brightness level for realizing gamma correction or other brightness weighting functions as desired (col. 17, lines 11-13, Bassetti).

Accordingly, Kudo et al and Bassetti teach all of the claimed limitations of claim 22, except for "a segment electrode driver circuit...using an orthogonal function which is specified by a scan pattern for four lines of common electrodes selected simultaneously by a multi-line drive method."

However, Hirai et al teaches a display device comprising an orthogonal transform of the column driver 80 with the j th column vector of the selection matrix is applied as a signal to a specified column electrode at the time of selecting the i-th simultaneously selected 4 row, recited at col. 24, lines 10-29.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to provide the orthogonal transform of the column driver 80 of the selection matrix is applied as a signal to a specified column electrode at the time of selecting the i-th simultaneously selected 4 row for Kudo's driver circuit (fig. 48), in view of the teaching in Hirai's reference because this would improve the picture image being displayed, while fabricating the driver circuits at low cost as taught by Hirai (col. 5, lines 57-63).

13. As to claim 25, see rejection of claim 5.

14. As to claim 26, Kudo et al teaches an upper display 500, and lower display 501 (fig. 48) including inherent a plurality of common electrodes and a plurality of segment electrodes which mutually intersect a plurality of pixels. Row drivers (502, 503) (figure 48) drive the segment electrodes.

Allowable Subject Matter

15. Claim 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

16. Applicant's arguments with respect to claims 1-23, 25, and 26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KN
December 28, 2004

XIAO WU
PRIMARY EXAMINER